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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,643	07/25/2000	Noriaki Hiraga	052593-5003	7356

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EXAMINER
KITOV, ZEEV

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 09/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,643	HIRAGA, NORIAKI	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 11,15, 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 3, 5 - 8* is/are rejected.

7)☒ Claim(s) *10,11,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. Applicant's Amendment made Claims 1 and 5 more definite, thus making examination possible. However, the Amendment to the Claims required a new search and a new ground for rejection was found. Applicant's arguments with respect to claims 1 – 11, 15 and 16 have been considered but are moot in view of the new ground(s) of rejection.

1. Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 3 and 5 - 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigemoto (US 5,923,570) in a view of Andersen et al. (US 6,147,538). Regarding Claims 1 and 5, Shigemoto discloses a clock wiring design having an inter-circuit wire (elements 18a, 18b and 18c in Fig. 1) interconnecting the internal circuits (elements A1, A2, B1, B2, C1, C2 in Fig. 1), which is not directly connected to the external signal input/output circuits. Internal circuit wires 18a, 18b and 18c are isolated from external environment by buffers 20a, 20b and 20c. It further discloses a plurality of internal circuits (elements A1, A2, B1, B2, C1 and C2 in Fig. 1).

However it does not disclose the rest of the elements of the claim associated with an ESD protection circuit. Andersen et al. discloses the ESD protection circuit including a an input/output connection (signal pad 113 in Fig. 3), a circuit arranged internally in a circuit forming region having different power supply lines (Vss in Fig. 3, while another supply line, Vdd, is inherent in the functional principle of the circuit), an active element in a first connection configuration connected to the inter-circuit signal wire (element N2, which is connected to the signal pad 113 in Fig. 3), plurality of other active elements in a second connection configuration including elements of an identical structure to the active element in the first connection configuration (element N1 in Fig. 3, which is shown in Fig. 5 as plurality of elements N1), these elements in the second connection configuration are being arranged adjacent to the active element in the first connection configuration sandwiching the latter (shown in Fig. 5), gates of the plurality of active elements in the second connection configuration being connected only to power lines (ground terminal in Fig. 3). Andersen et al. further disclose a plurality of the internal circuits, which implicitly have the same power supply lines.

Both patents have the same problem solving area, namely design of semiconductor integrated circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Shigemoto solution by adding the Andersen et al. ESD protection circuit, because as Andersen et al. state (col. 1, line 11 – col. 2, line 15), the semiconductor IC's, especially modern MOS technology are highly vulnerable to the ESD events and must be protected from them.

Regarding Claims 3 and 8, Andersen discloses a substrate formed in a single chip, wherein the circuit-forming region is allocated to one side of the substrate (see Fig.5). A motivation for modification of a primary reference is the same as above.

Regarding Claim 6, Andersen discloses a plurality of the active elements in the second connection configuration (elements N1 in Fig. 3 and 4) arranged to sandwich the active element in the first connection configuration (element N2 in Fig. 3, and Fig. 5). A motivation for modification of a primary reference is the same as above.

Regarding Claims 2 and 7, Shigemoto discloses a plurality of basic cells regularly arranged in repetition (elements 18a, 18b and 18c in Fig. 1). As to active elements in the first and second connection configurations allocated to some of the basic cells, as well known in the art, possibility of an ESD imposed onto voltage supply busses requires use of active protection means. Accordingly, the Andersen ESD protection circuit is the one that can be efficiently used for that purpose. Both patents have the same problem solving area, namely ESD protection of semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied the Andersen ESD protection solution to the Shigemoto clock distribution structure, because as Andersen states (col. 1,line 11 – col. 2, line 15), the semiconductor IC's, especially modern MOS technology are highly vulnerable to the ESD events and must be protected from them.

2. Allowabl Subj ct Matter

Claims 10, 11, 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

A reason for that is as follows. In claim 10, an Applicant discloses, inter alia, an active element in a third connection configuration arranged adjacent to the active element in the first connection configuration. Even though a reference with such active element in the third connection configuration can be found, there is no obvious motivation for introducing such element, which is supposed to be interleaved with the element in the first connection configuration. Accordingly, all other claims 11, 15 and 16 become allowable, since they are dependent on Claim 10.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

3. Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone numbers for organization where this application or proceedings is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
08/15/2003

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800